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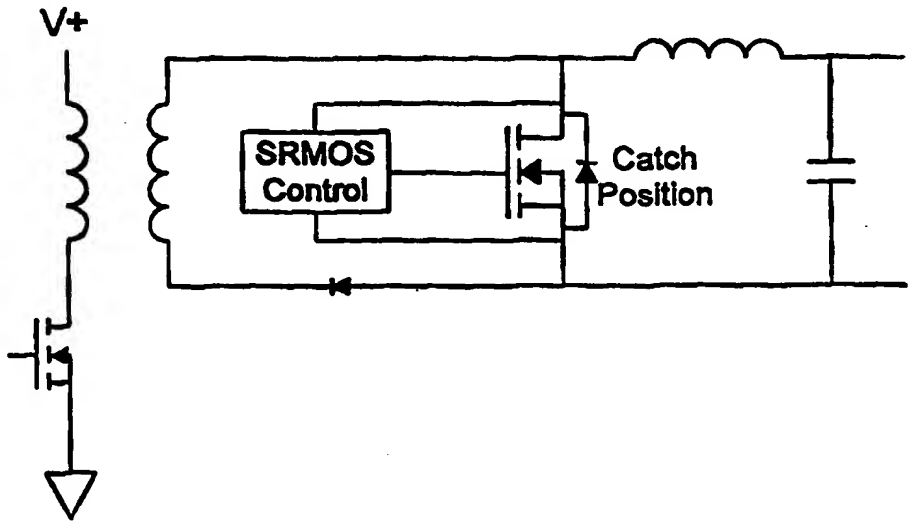

(57) Abstract

Circuits and methods are provided for operating a transistor as rectifier based upon the detected Vds of the transistor. In sensing the Vds v ltage of the SRMOS, during positive conduction, the SRMOS body diode will conduct and the Vds of the SRMOS becomes that f a forward body diode voltage, which may, depending on the type of the device, be approximately – 0.6 V. If this v ltage level is sensed, it may indicate that the SRMOS is turned off too early. During reverse conduction, Vds is non-existent (which is similar to a diode). In this case, the SRMOS may be turned off too late. Thus, by xamining Vds, the SRMOS can be operated in such a manner so that it is turned off at an optimal point in time.

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Specification

METHOD AND CIRCUIT FOR OPERATING A TRANSISTOR AS A RECTIFIER

BACKGROUND OF THE INVENTION

PRIORITY CLAIM

This application claims priority to a provisional application entitled "SRMOS Control in DC/DC Power Converters" filed on June 2, 1997, having an Application Number 60/048,288.

Field of the Invention

The present invention generally relates to electrical rectifying circuits and, in particular, to rectifying circuit that uses a transistor as a rectifier.

Description of the Prior Art

In power converters, synchronous rectifier MOS (SRMOS) transistors are used and operated in such a manner to perform like a diode, allowing conduction in one direction and preventing conduction in the opposite direction. The advantage with using an SRMOS transistor in the place of a diode is the higher efficiency obtainable with an SRMOS -- namely the avoidance of the voltage drop across a conventional diode. This advantage becomes increasing important as greater demand and operation time is demanded from a limited power source such as batteries. In the case of a converter circuit, it becomes even more crucial that there is minimal voltage drop in converting one voltage level to another voltage level. Otherwise, a great deal of power would be lost in the conversion process itself.

Traditionally, SRMOS are controlled by several methods. Referring to Fig. 1a, a prior art converter circuit with a SRMOS is illustrated. This circuit is comprised of a first transistor 10 having gate, drain and source terminals, and the transistor is connected at one terminal to a voltage source having a particular voltage level and is connected at another terminal in series to a coil 12, and to a capacitor 16. A second transistor 18, being operated as a synchronous rectifier (SRMOS), is connected at one terminal to a node between the first transistor 10 and the coil 12 and is connected at another terminal to the common ground terminal. A pulse width

modulation (PWM) control circuit 20, having a probe at the output terminal 22, detects the output voltage level. The PWM control circuit operates transistors 10 and 18 in response to the detected voltage level and causes the generation of the desired voltage level at the output terminal. Transistors 10 and 18 are controlled by a common signal and transistor 18 is connected via an inverter 14. When transistor 10 is turned on, transistor 18 is turned off. In some cases, an optional external diode is placed across transistor 10.

In this type of circuit, referring to Fig. 1b illustrating the gate voltage for transistor 10 (which is being operated as the main switch for generating the desired output voltage level) and Fig. 1c illustrating the gate voltage in operating the SRMOS (transistor 18) and Fig. 1d illustrating the current in the inductor 12, the SRMOS (transistor 18) is turned on whenever the main converter switch (transistor 10) is turned off (as indicated at 24), and the SRMOS (transistor 18) is turned off whenever the main converter switch (transistor 10) is turned on. While this is a simple arrangement, when the SRMOS is turned on, there is a large amount of reverse conduction (current flow indicated at 28) that reduces overall converter efficiency.

In yet another prior art circuit, referring to Fig. 2a, a SRMOS converter circuit using the current sense control method is illustrated. This circuit is comprised of a first transistor 30 having gate, drain and source terminals, where the transistor is connected at one terminal to a voltage source having a particular voltage level and is connected at another terminal in series to a coil 32, a shunt 34 (for current sensing), and a capacitor 36. A second transistor 38, being operated like a synchronous rectifier, is connected at one terminal to a node between the first transistor 30 and the coil 32 and is connected at the other terminal to the common ground terminal. A pulse width modulation (PWM) control circuit 40, having two probes for current sensing across the shunt 34 and a probe at the output terminal 42, detects the current level and the output voltage level. The PWM control circuit operates transistors 30 and 38 in response to the detected voltage and current levels and causes the generation of the desired voltage level at the output terminal 42.

In this type of circuit, referring to Fig. 2b illustrating the timing of the gate voltage for transistor 30 and Fig. 2c illustrating timing of the gate voltage in operating the SRMOS (transistor 38) and Fig. 2d illustrating current flow of the inductor, in the discontinuous mode when there is reverse conduction and the inductor current starts to flow in the negative direction through the SRMOS (transistor 38), current flow is sensed through the use of the shunt 34. The control circuit 40 sensing reverse conduction turns off the SRMOS (transistor 38) to prevent further reverse conduction. However, since the shunt resistance is typically very small, it is

difficult to precisely detect the timing of the zero crossing of the current. Thus, the SRMOS is turned off either before the zero crossing or after the zero crossing, rendering this an imprecise method. Because this is an imprecise method, there still may be a large amount of negative current flow (as indicated in Fig. 3d, 48). Additionally, the shunt is a resistor which consumes power as well (lossy). While the typical shunt resistor is 33mΩ and the power consumption can be reduced by using a shunt with even smaller resistance, with a smaller shunt, there will be more reverse conduction before the negative current can be detected. Overall, this circuit is not a reliable nor efficient converter circuit.

In still yet another prior art circuit, referring to Fig. 3a, a SRMOS converter circuit using Vds sensing control method is illustrated. This circuit is comprised of a first transistor 50 having gate, drain and source terminals, where the transistor is connected at one terminal to a voltage source having a particular voltage level and is connected at another terminal in series to a coil 52, and the coil is connected to a capacitor 56. A second transistor 58, being operated like a synchronous rectifier, is connected at one terminal to a node between the first transistor 50 and the coil 52 and is connected at the other terminal to the common ground terminal. A pulse width modulation (PWM) control circuit 60, having a probe 54 for voltage sensing at a node between transistor 50 and coil 52 and a probe at the output terminal 62, detects the Vds level and the output voltage level. The PWM control circuit operates transistors 50 and 58 in response to the detected voltage levels and causes the generation of the desired voltage level at the output terminal 62.

Fig. 3b illustrates the timing of the gate voltage for transistor 50 of Fig. 3a, Fig. 3c illustrates timing of the gate voltage in operating the SRMOS (transistor 58) in view of the Fig. 3b, and Fig. 3d illustrates current flow of this circuit. In this type of circuit, in the discontinuous mode when there is reverse conduction and the inductor current starts to flow in the negative direction through the SRMOS (transistor 58), the SRMOS drain voltage (Vds) becomes positive which is sense by the control circuit 60 and the control circuit turns the SRMOS off. However, in practice, precise Vds sensing is difficult and reverse conduction occurs (as shown in Fig. 3d, 64), rendering this type of circuit unreliable and inefficient.

Given the state of the art and the demand for a more efficient converter circuit, it would be desirable to have a method and circuit that can perform rectifying function and prevent the occurrence of reverse conduction through the use of a transistor.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide circuits and methods for operating a transistor as a rectifier.

It is another object of the present invention to provide circuits and methods for operating a transistor as a rectifier using the Vds voltage potential of the transistor as an indicator.

It is yet another object of the present invention to provide circuits and methods for operating a transistor as a rectifier and preventing reverse conduction by said transistor while allowing forward conduction.

Briefly, circuits and methods are provided for operating a transistor as a rectifier based upon the detected Vds of the transistor. In sensing the Vds voltage of the SRMOS during the off-state. during positive conduction (of the transistor), the SRMOS body diode conducts and the Vds of the SRMOS becomes that of a forward body diode voltage, which may, depending on the type of the device, be approximately -0.6V. If this voltage level is sensed, it may indicate that the SRMOS is turned off too early. During reverse conduction, Vds is non-existent (which is similar to a diode). In this case, the SRMOS may be turned off too late. Thus, by examining Vds, the SRMOS can be operated in such a manner so that it is turned off at an optimal point in time.

An advantage of the present invention is that it provides circuits and methods for operating a transistor as a rectifier.

Another advantage of the present invention is that it provides circuits and methods for operating a transistor as a rectifier using the Vds voltage potential of the transistor as an indicator.

Yet another advantage of the present invention is that it provides circuits and methods for operating a transistor as a rectifier and preventing reverse conduction by said transistor while allowing forward conduction.

These and other features and advantages of the present invention will become well understood upon examining the figures and reading the following detailed description of the invention.

IN THE DRAWINGS

Fig. 1a illustrates a prior art SRMOS converter circuit using a simple switch method;

Fig. 1b illustrates the gate voltage for operating the main switch transistor of Fig. 1a;

Fig. 1c illustrates the gate voltage in operating the SRMOS of Fig. 1a;

Fig. 1d illustrates the current of the Fig. 1a circuit;

Fig. 2a shows a prior art SRMOS converter circuit using the current sense control method;

Fig. 2b illustrates the timing of the gate voltage in operating the main switch transistor of Fig. 2a;

Fig. 2c illustrates the timing of the gate voltage in operating the SRMOS of Fig. 2a;

Fig. 2d illustrates the current flow of the Fig. 2a circuit;

Fig. 3a illustrates a SRMOS converter circuit using Vds sensing control method;

Fig. 3b illustrates the timing of the gate voltage in operating the main switch transistor of Fig. 3a;

Fig. 3c illustrates the timing of the gate voltage in operating the SRMOS of Fig. 3a;

Fig. 3d illustrates the current flow of the Fig. 3a circuit;

Fig. 4a illustrates the Vds of the SRMOS of the preferred method of the present invention;

Fig. 4b illustrates the Vgs for operating the SRMOS of the preferred method in view of Fig. 4a;

Fig. 4c illustrates the reference voltage, Vref, for the preferred method of the present invention;

Fig. 5a illustrates Vramp and Vref of the preferred method showing the upward adjustment of Vref;

Fig. 5b illustrates Vgs of the SRMOS in relation with the intersection of Vramp and Vref of Fig. 5a of the preferred method;

Fig. 6a shows the intersection of Vds and Vref for turning off of the SRMOS on the upward slope of the Vds;

Fig. 6b illustrates that when Vref and Vds are at the same level Vgs is applied to turn off the SRMOS;

Fig. 7a shows that the duration of the SRMOS on-time is reduced as the load is reduced;

Fig. 7b shows that an increase in the duration of diode conduction indicates an increased load and the on-time of the SRMOS Vgs is increased to handled the increased load;

Fig. 8a illustrates one circuit embodiment for a buck DC/DC converter of the present invention;

Figs. 8b, 8c, and 8d illustrate the relationship between Vgs of the main switch transistor, Vgs of the SRMOS transistor, and current flow of the circuit showing no reverse conduction;

Fig. 9 illustrates an embodiment for the control circuit to control the SRMOS;

Figs. 10a and 10b illustrate the adjustment of Vref when there is a rapid change in load; and

Figs. 11-13 illustrate applications of the present invention in converter circuits.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In a presently preferred embodiments of the present invention, an adaptive predicted SRMOS control method and an adaptive Vds sensing SRMOS control method are disclosed. By using either of these methods, reverse conduction is significantly reduced or even eliminated. In each method, a reference voltage is provided and adjusted so that the SRMOS is turned off optimally when there is very short body diode conduction and no reverse conduction.

A MOSFET transistor operated as a rectifier is referred to as a SRMOS. During the off-state of the transistor, there is no current going from the drain terminal to the source terminal. However, there can be a voltage difference across the two terminals (Vds). If the voltage potential at the drain terminal is higher than the voltage potential at the source terminal, Vds voltage would be the difference between the two voltage potentials. If the voltage potential at the source terminal is higher than the voltage potential at the drain terminal, Vds voltage would be the forward body diode voltage of the transistor or that of an external diode if an external diode is connected across the two terminals.

More specifically, in sensing the Vds voltage of the SRMOS, during positive conduction (current going from source to drain), the SRMOS body diode will conduct and the Vds of the SRMOS becomes that of a forward body diode voltage of the transistor or of that of a connected external diode, which may, depending on the type of the device, be approximately -0.6V. If this voltage level is sensed, it may indicate that the SRMOS is turned off too early. During reverse conduction (current going from drain to source), Vds is near-zero. In this case, the SRMOS may be turned off too late. Thus, by examining Vds, the SRMOS can be operated in such a manner so that it is turned off at an optimal point in time.

A reference voltage for determining the timing in turning off the SRMOS is provided to accurately gauge the turn-off time for the SRMOS. The reference voltage can be provided by using a capacitor voltage where the capacitor voltage is increased to delay the SRMOS turn-off time when a Vds forward body diode voltage is detected and the capacitor voltage is decreased to turn off the SRMOS earlier in time when no Vds forward body diode voltage is detected or the duration of a detected forward body diode voltage is shorter than a predefined time period.

Referring to Figs. 4a, 4b, and 4c, Fig. 4a illustrates Vds of the SRMOS, Fig. 4b illustrates the Vgs in operating the SRMOS, and Fig. 4c illustrates reference voltage, Vref. Referring to Figs. 4a, 4b and 4c, the SRMOS is turned off too early in time (by applying Vgs as indicated at 72) such that a diode conduction (as indicated at 70) occurs (Vds approximately equals to the forward body diode voltage). When the reference voltage is adjusted upwards (as indicated at 74), the SRMOS is turned off at a later point in time (as indicated at 78), resulting in minimal diode conduction 76.

In determining the point in time to turn off the SRMOS, in one method the reference voltage is compared against a periodic ramp voltage (Vramp). When Vramp exceeds Vref, a signal is generated to turn off the SRMOS. The ramp voltage can be generated in one of several ways. It can be generated as a function of the PWM signal, the Vds signal of the SRMOS, or in other manners.

In using a generated or PWM ramp voltage in conjunction with the reference voltage, a time-based, predicted SRMOS turn off signal can be generated where this signal is based upon the previous SRMOS timing. If the converter duty cycle quickly changes, a few cycle is required to adjust Vref in relation with Vramp for turning off the SRMOS. Fig. 5a illustrates Vramp and Vref showing the upward adjustment of Vref. Fig. 5b illustrates the Vgs of the SRMOS in relation with the intersection of Vramp and Vref of Fig. 5a. As Vref is upwardly adjusted on Vramp, Vgs is prolonged and the SRMOS on-time is increased (82), and as Vref is downwardly adjusted on Vramp, Vgs is shortened and the SRMOS on-time is decreased (80).

In the adaptive Vds sensing SRMOS control method, referring to Fig. 6a illustrating Vds and Vref, the reference voltage is compared with Vds and the SRMOS is turned off when Vref, on the upward slope of the Vds (as indicated at 84), meets Vref (as indicated at 86). Referring to Fig. 6b, when Vref and Vds are the same (as Vds increases in value), Vgs is applied to turn off the SRMOS (as indicated at 88). In this method, no ramp voltage is necessary. The reference voltage is provided so that the circuit does not need to precisely determine the zero-crossing point. Additionally, any component offset voltage resulting from the manufacturing process or operating conditions can be accounted for by adjusting the reference voltage.

Once the SRMOS turn-off time is optimal, the on-time of the SRMOS can be used to determine the load condition of the converter. When the load condition is known, other power saving techniques can be applied to further optimize converter output.

In detecting the load condition, at full load the SRMOS will remain on until the main converter switch is turned on. As the load decreases, the SRMOS turns off before the main

converter switch is turned on. Therefore, the on-time of SRMOS indicates the load condition. Once the load condition is known, other power saving methods can be used. For example, in light load condition, the amount of on-time of the main converter switch (and/or the SRMOS) can be reduced, the SRMOS function can be replaced with the body diode or external diode, and the converter operating frequency can be reduced. Referring to Fig. 7a, the duration of the SRMOS on-time is reduced as indicated at 90 and 92 as the load is reduced. On the other hand, referring to Fig. 7b, an increase in the duration of diode conduction (as indicated at 94) indicates an increased load and the on-time of the SRMOS Vgs can be increased to handled the increased load.

Fig. 8a illustrates one circuit embodiment for a buck DC/DC converter of the present invention where the methods for operating the SRMOS (transistor 108) are novel and can be embedded in the PWM control circuit. The methods described herein can be used in buck, boost, and other types of converters. Figs. 8b, 8c, and 8d illustrate the relationship between Vgs of transistor 100. Vgs of transistor 108, and current flow of the circuit which shows no reverse conduction.

Fig. 9 illustrates one embodiment of the PWM control circuit for the present invention. A comparator 120 compares the detected Vds and ground to determine the existence of Vds at the level of a forward diode voltage potential. If Vds equals the forward body diode voltage for a duration longer than a first predefined time period (122), the reference voltage described above (Vref) is increased (124). If Vds equals the forward body diode voltage for a duration less than a second predefined time period (126), the reference voltage is decreased (128). Vref 130 is then compared to another signal at comparator 132. The other signal, depending on the embodiment, can be from one of two possible methods. In the adaptive, predicted SRMOS control method as described above, there is a ramp voltage Vramp and Vramp is used as an input to the comparator 132. In the adaptive Vds sensing SRMOS control method described above, Vds is used as an input to the comparator 132. In either case, if Vref equals to the provided signal (either Vramp or Vds), a signal is provided to the Off-Driver 138 for the SRMOS to turn off the SRMOS.

In a situation where there is a rapid change in converter load, the prediction circuit may not be able to adjust to this rapid change, and reverse conduction may result. In order to provide for this situation, in yet another aspect of the present invention and referring to Figs. 10a and 10b, the SRMOS Vds and Vgs voltages are examined and compared. If the falling edge of Vgs is ahead of the rising edge of Vds for less than some predetermined amount of time 150, the reference voltage is quickly reduced 152.

Figs. 11-13 illustrates application of the present invention in alternative circuit configurations. Referring to Fig. 11 illustrating a forward converter, the SRMOS transistor is placed in the catch position of the converter circuit and it is controlled in such a manner so that it is on for the optimal maximum duration while avoiding reverse conduction. Fig. 12 illustrates another forward converter configuration where the SRMOS transistor is placed in the forward position. With this configuration, the forward converter avoids reverse conduction and can be used in parallel converter applications. Referring to Fig. 13, the present invention enables the use of a SRMOS in a flyback converter where traditionally SRMOS are not easily implemented.

It is important to note that the present invention can be used in a variety of applications including periodic switching applications, and it is not limited to converters or the embodiments described herein. Furthermore, the methods described herein can be used in conjunction with prior art methods. For example, the current across the drain and source terminals of the SRMOS transistor can be sensed for reverse current flow, and the prediction methods and circuits (e.g. ramp voltage and reference voltage) of the present invention can be adapted to adjust the operation of the SRMOS so that the transistor is operated in such a manner so there is no reverse current flow in subsequent cycles. More specifically, the reference voltage can be adjusted on one hand by detecting for reverse current flow when there is reverse current flow and for Vds at a diode voltage when there is no reverse current flow but the transistor is turned off too early.

Moreover, although the description provides for the adjustment of the reference voltage with respect to the ramp voltage or the adjustment of the reference voltage with respected to the Vds voltage, it is entirely within the teaching of the present invention to provide for other types of reference voltage combinations for operating the SRMOS transistor, including the adjustment of the ramp voltage rather than the reference voltage and the use and adjustment of other types of voltage signals such a saw-tooth signal.

While the present invention has been described with reference to certain preferred embodiments, it is to be understood that the present invention is not to be limited to such specific embodiments. Rather, it is the inventor's intention that the invention be understood and construed in its broadest meaning as reflected by the following claims. Thus, these claims are to be understood as incorporating and not only the preferred embodiment described herein but all those other and further alterations and modifications as would be apparent to those of ordinary skill in the art.

What I claim is:

CLAIMS

1. A circuit for operating a transistor as a rectifier, said circuit comprising:

a transistor;

a control circuit operating said transistor as a function of the Vds voltage potential of said transistor.

2. A circuit as recited in claim 1 wherein said transistor is a MOSFET.

3. A circuit as recited in claim 1 wherein a reference signal is provided.

4. A circuit as recited in 3 wherein said reference signal has a voltage potential in the same range as the voltage potential of the Vds voltage of said transistor.

5. A circuit as recited in claim 4 wherein said control circuit adjusts said reference signal upward when said detected Vds voltage is at a diode voltage potential for a duration greater than a first predefined time period.

6. A circuit as recited in claim 5 wherein said diode voltage potential is the forward body diode voltage of said transistor.

7. A circuit as recited in claim 5 wherein said diode voltage potential is the forward diode voltage of an external diode connected across the drain and source terminals of said transistor.

8. A circuit as recited in claim 4 wherein said control circuit adjusts said reference signal downward when said detected Vds voltage is at a diode voltage potential for a duration less than a second predefined time period.

9. A circuit as recited in claim 8 wherein said diode voltage potential is the forward body diode voltage of said transistor.

10. A circuit as recited in claim 8 wherein said diode voltage potential is the forward diode voltage of an external diode connected across the drain and source terminals of said transistor.

11. A circuit as recited in claim 3 wherein a periodic ramp voltage is provided.

12. A circuit as recited in claim 11 wherein when the voltage potential of said ramp voltage and said reference voltage are at the same level, said transistor is operated.

13. A circuit as recited in claim 12 wherein said control circuit adjusts said reference signal upward when said detected Vds voltage is at a diode voltage potential for a duration greater than a first predefined time period.

14. A circuit as recited in claim 13 wherein said diode voltage potential is the forward body diode voltage of said transistor.

15. A circuit as recited in claim 13 wherein said diode voltage potential is the forward diode voltage of an external diode connected across the drain and source terminals of said transistor.

16. A circuit as recited in claim 12 wherein said control circuit adjusts said reference signal downward when said detected Vds voltage is at a diode voltage potential for a duration less than a second predefined time period.

17. A circuit as recited in claim 16 wherein said diode voltage potential is the forward body diode voltage of said transistor.

18. A circuit as recited in claim 16 wherein said diode voltage potential is the forward diode voltage of an external diode connected across the drain and source terminals of said transistor.

19. A circuit as recited in claim 12 wherein operating said transistor to turn off said transistor.

20. A circuit as recited in claim 1 wherein said transistor is turned off earlier in a second cycle if in a first cycle said transistor is off for a duration less than a predefined third time period.

21. A method for operating a transistor as a rectifier, comprising the steps of:

detecting the Vds voltage of a transistor;

operating said transistor as a function of the duration of said detected Vds voltage in the range of a diode voltage potential.

22. A method as recited in claim 21 wherein said diode voltage is the forward body diode voltage of said transistor.

23. A method as recited in claim 21 wherein said diode voltage is the forward voltage of an external diode connected across the drain and source terminals of said transistor.

24. A method as recited in claim 21 wherein in said operating step, said transistor is operated at a later point in time in a subsequent cycle if said detected Vds voltage is at a particular diode voltage potential for duration greater than a first predefined time period.

25. A method as recited in claim 21 wherein in said operating step, said transistor is operated at an earlier point in time in a subsequent cycle if said detected Vds voltage is at a particular diode voltage potential for duration less than a second predefined time period.

26. A method as recited in claim 21 wherein a reference voltage is provided.

27. A method as recited in claim 26 wherein said reference voltage is adjusted as a function of said detected Vds voltage.

28. A method as recited in claim 27 wherein said transistor is operated when said reference voltage and said detected Vds voltage of said transistor are in the same voltage potential range.

29. A method as recited in claim 28 wherein said reference voltage is adjusted upward when the Vds voltage of said transistor is at a diode voltage for a duration greater than a first predefined time period.

30. A method as recited in claim 28 wherein said reference voltage is adjusted downward when the Vds voltage of said transistor is at a diode voltage for a duration less than a second predefined time period.

31. A method as recited in claim 26 wherein a ramp voltage is provided.

32. A method as recited in claim 31 wherein said reference voltage is adjusted as a function of said detected Vds voltage.

33. A method as recited in claim 32 wherein said transistor is operated when said reference voltage and said ramp voltage are in the same voltage potential range.

34. A method as recited in claim 33 wherein said reference voltage is adjusted upward when the Vds voltage of said transistor is at a diode voltage for a duration greater than a first predefined time period.

35. A method as recited in claim 33 wherein said reference voltage is adjusted downward when the Vds voltage of said transistor is at a diode voltage for a duration less than a second predefined time period.

36. A method as recited in claim 21 wherein said transistor is turned off earlier in a second cycle if in a first cycle said transistor is off for a duration less than a predefined third time period.

37. A method for operating a transistor as a rectifier, comprising the steps of:

generating a periodic ramp signal;

providing a reference signal having a particular voltage potential;

detecting for reverse current flow through said transistor;

adjusting said reference signal as a function of said detected reverse current flow;

operating said transistor when said reference signal and said ramp signal are at the same voltage potential.

38. A method as recited in claim 37 wherein said ramp signal is generated as a function of the switching frequency of a converter circuit.

39. A method as recited in claim 37 further including before the adjusting step the step of detecting for Vds voltage of said transistor.

40. A method as recited in claim 39 wherein said adjusting step adjusts said reference voltage as a function of said detected reverse current flow and said detected Vds voltage of said transistor.

41. A method as recited in claim 40 wherein in said adjusting step, said reference signal is adjusted downward if said detected reverse current flow is detected.

42. A method as recited in claim 39 wherein in said adjusting step, said reference signal is adjusted upward if said detected Vds voltage is at a particular diode voltage potential for duration greater than a first predefined time period.

43. A method as recited in claim 42 wherein said particular diode voltage potential is the forward body diode voltage of said transistor.

44. A method as recited in claim 42 wherein said particular diode voltage potential is the forward diode voltage of an external diode connected across the drain and source terminals of said transistor.

45. A method as recited in claim 37 wherein in said operating step said transistor is turned off.

46. A method as recited in claim 37 wherein said transistor is turned off earlier in a second cycle if in a first cycle said transistor is off for a duration less than a predefined third time period.

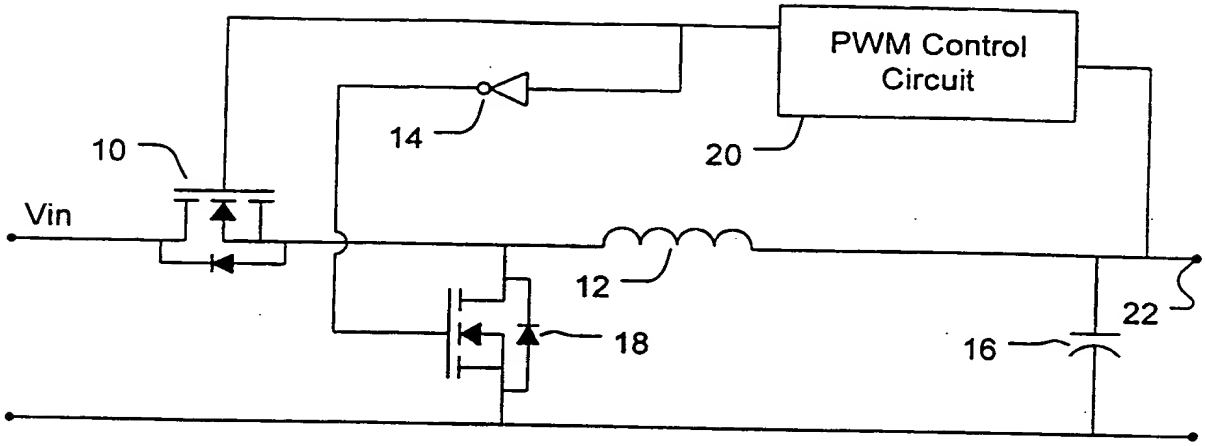

Fig. 1a
(Prior Art)

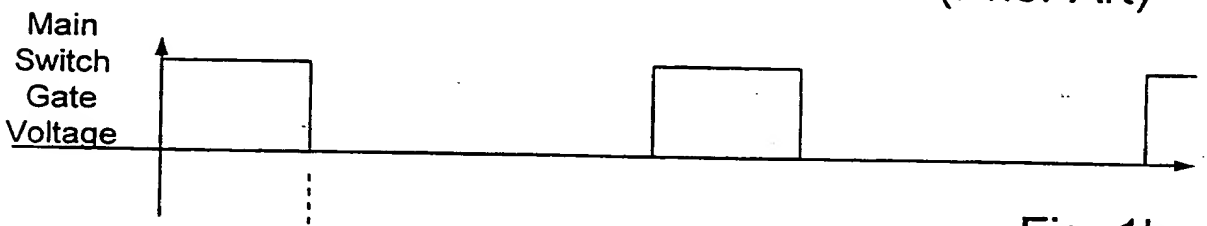

Fig. 1b

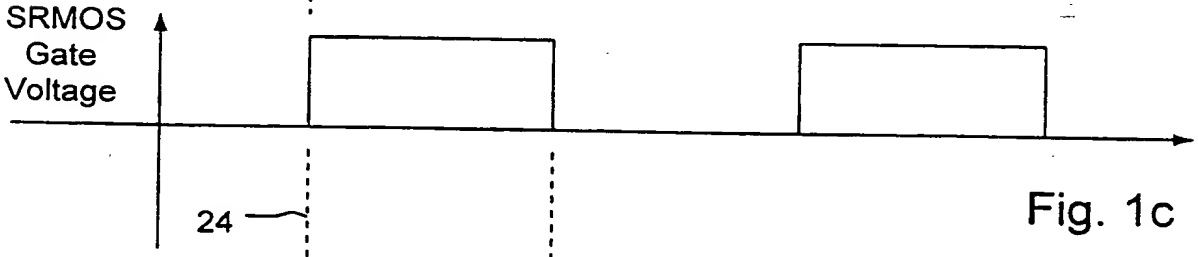

Fig. 1c

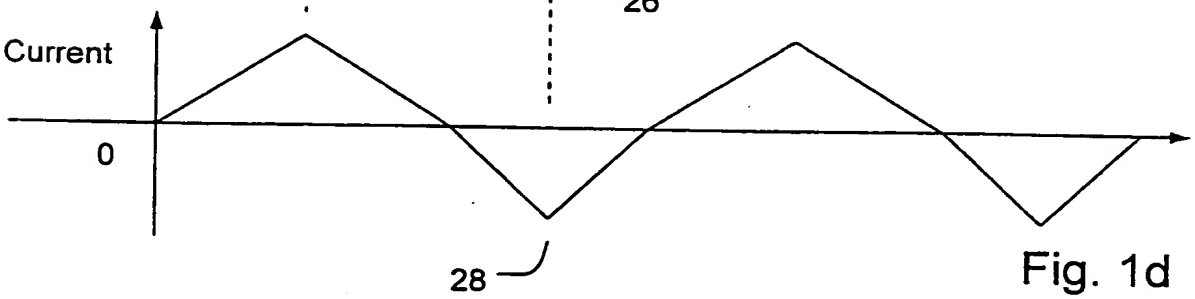

Fig. 1d

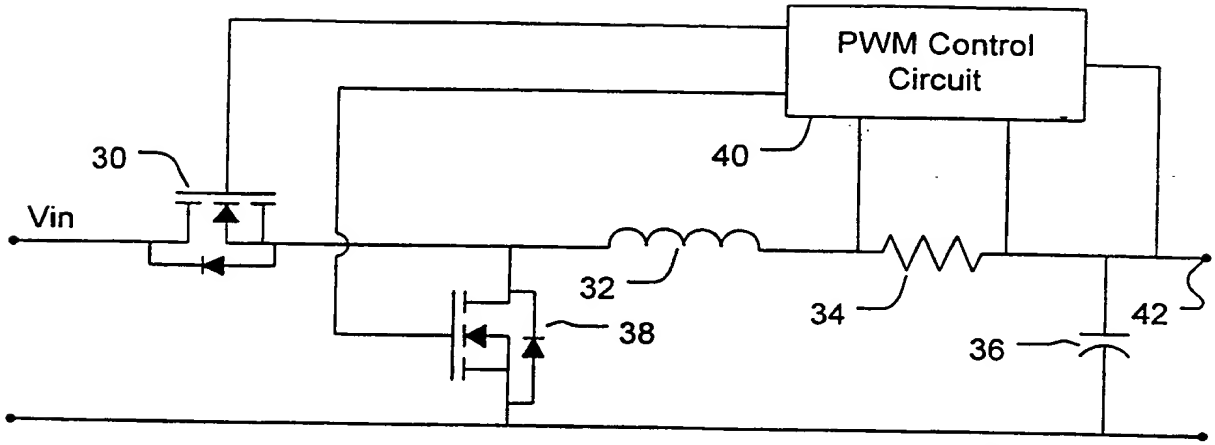

Fig. 2a
(Prior Art)

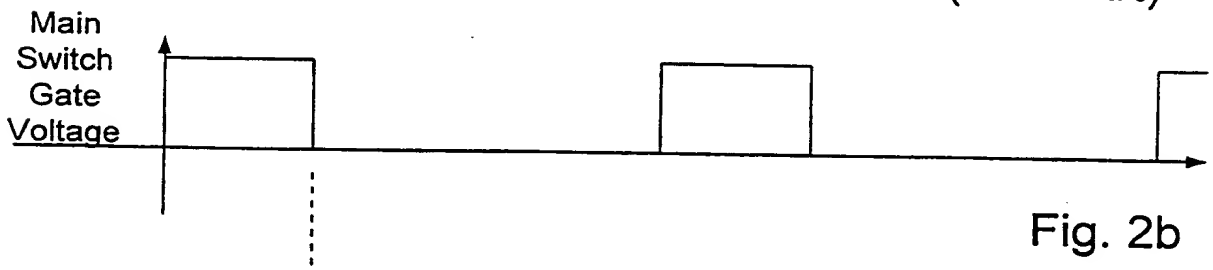

Fig. 2b

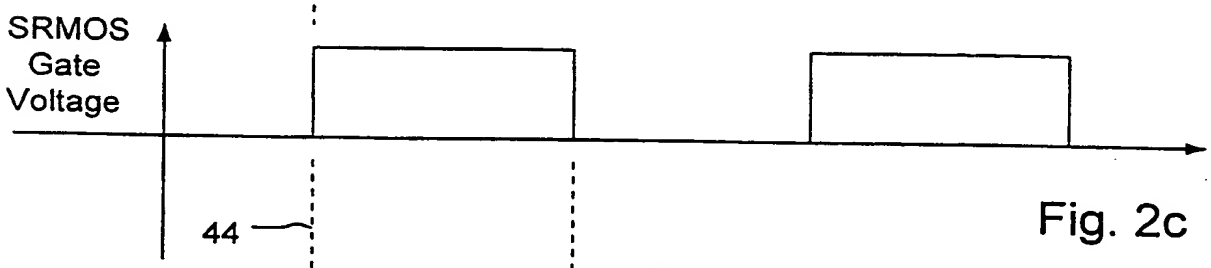

Fig. 2c

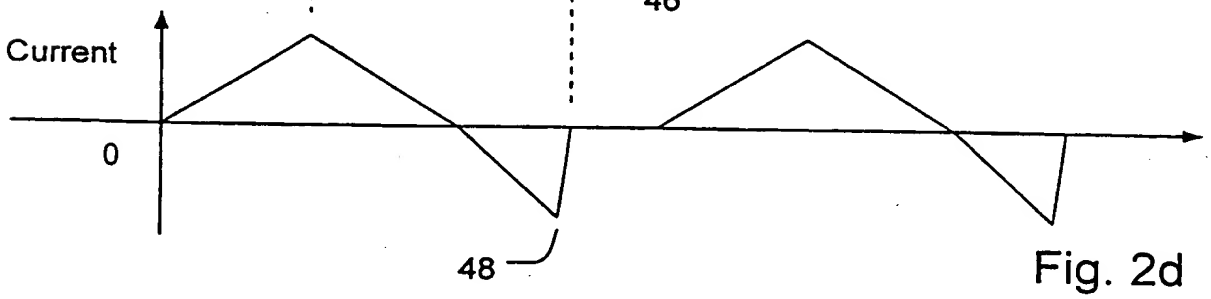

Fig. 2d

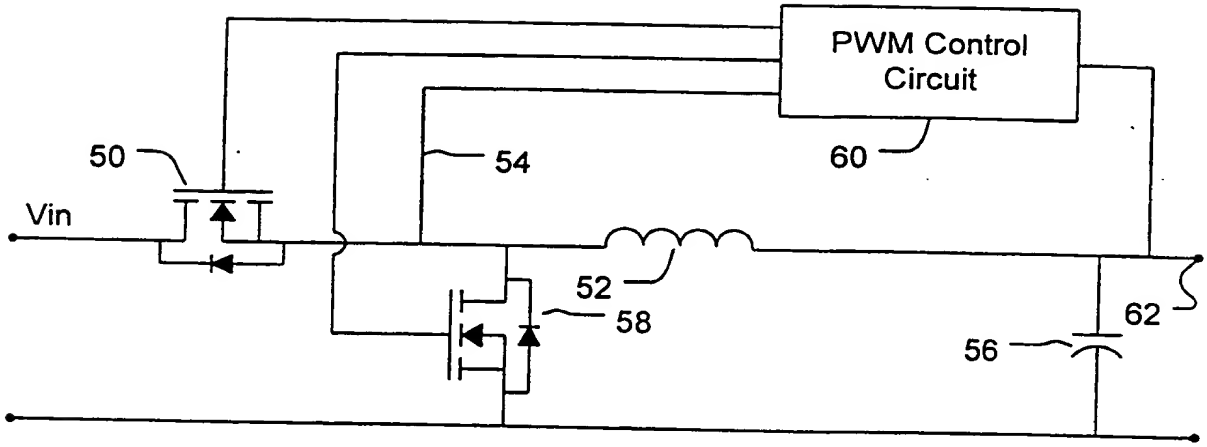

Fig. 3a
(Prior Art)

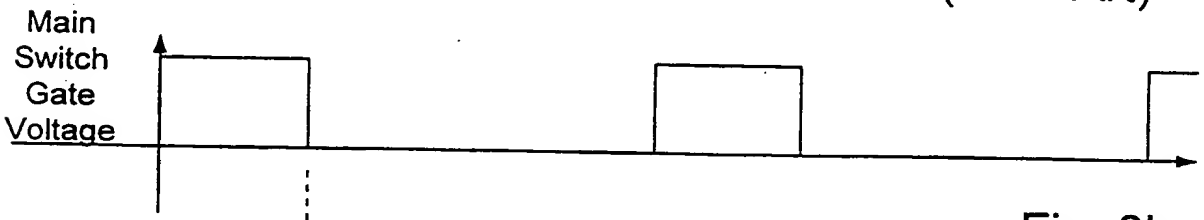

Fig. 3b

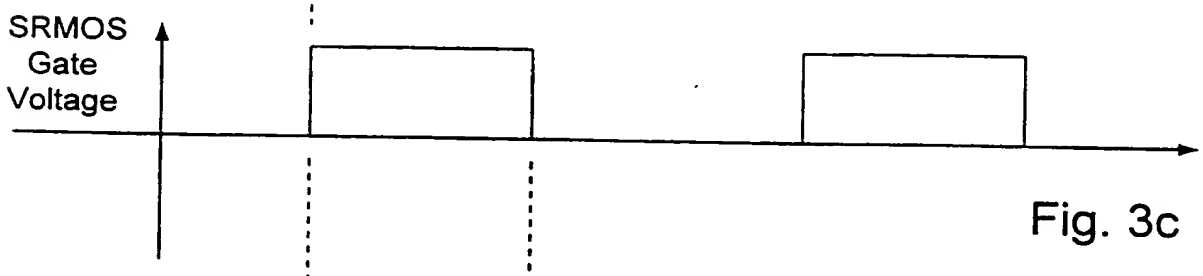

Fig. 3c

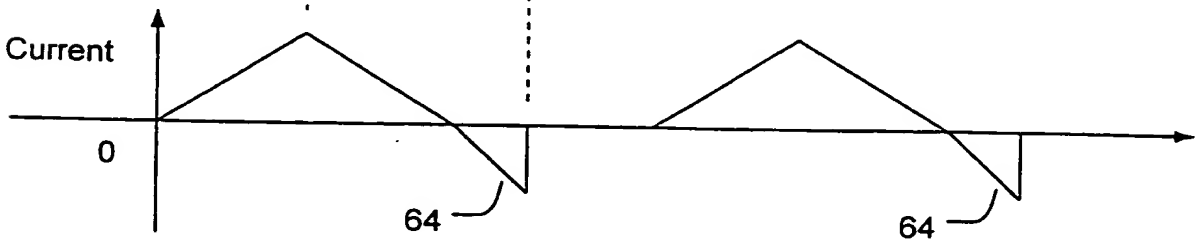

Fig. 3d

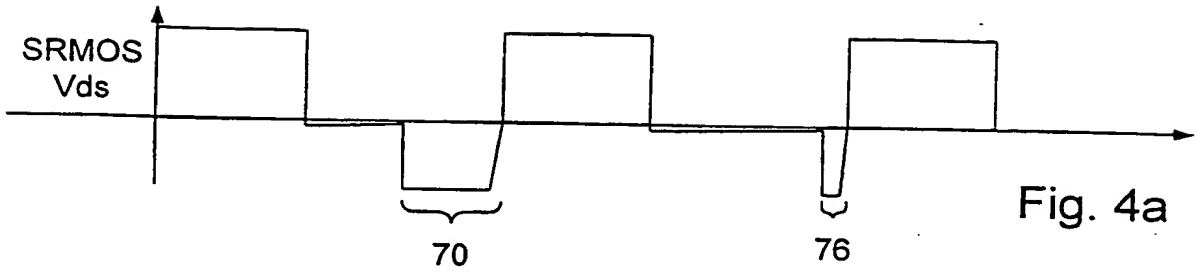

Fig. 4a

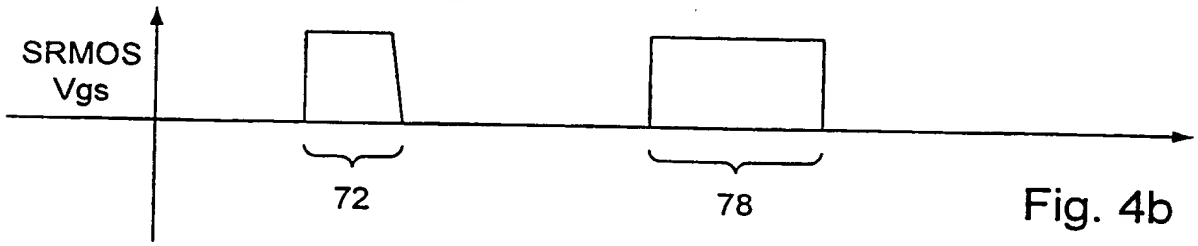

Fig. 4b

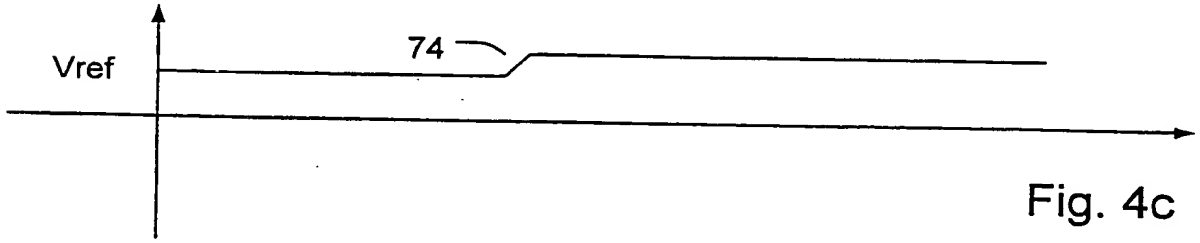

Fig. 4c

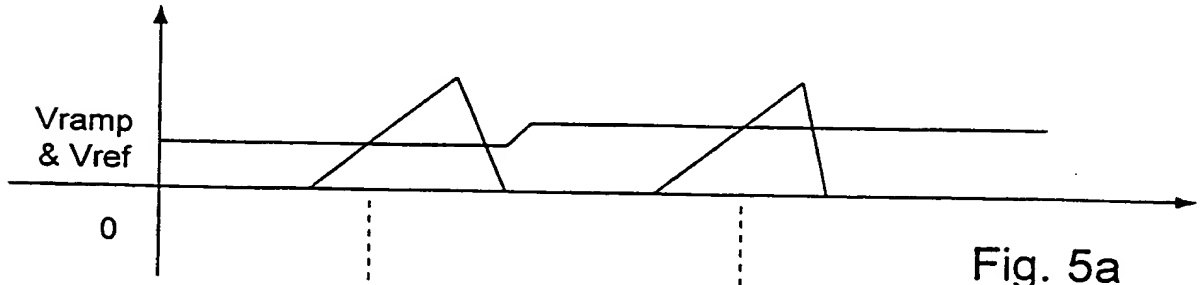

Fig. 5a

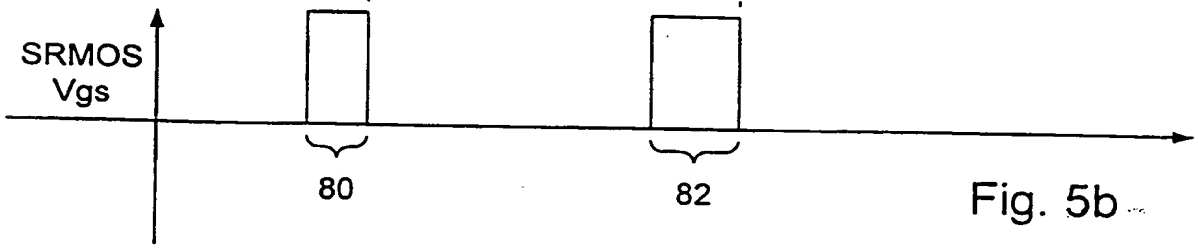

Fig. 5b

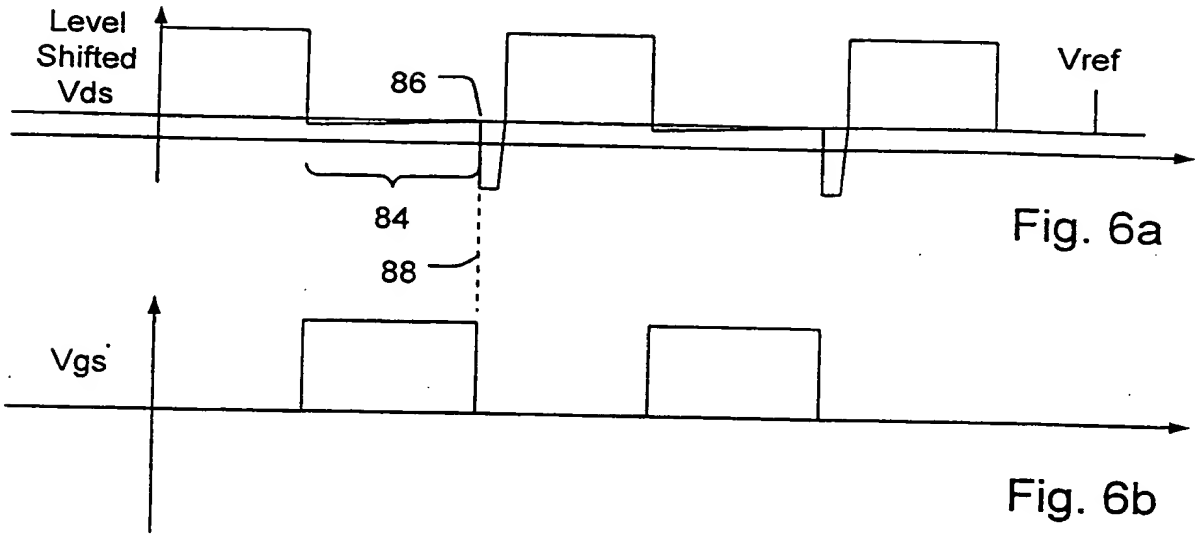

Fig. 6a

Fig. 6b

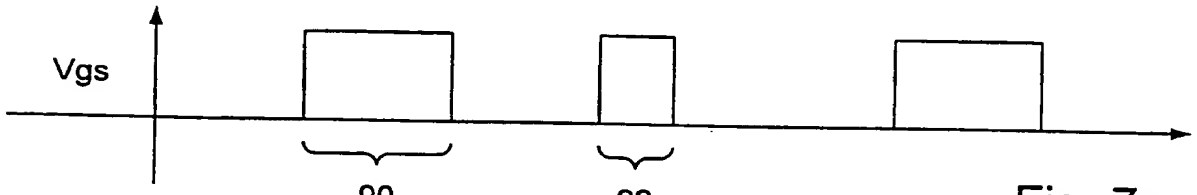

Fig. 7a

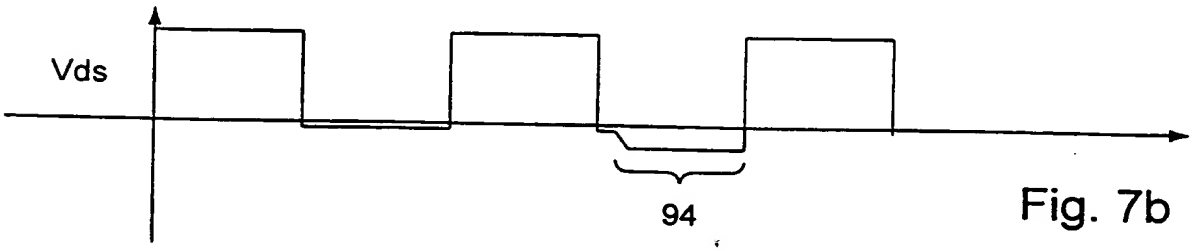

Fig. 7b

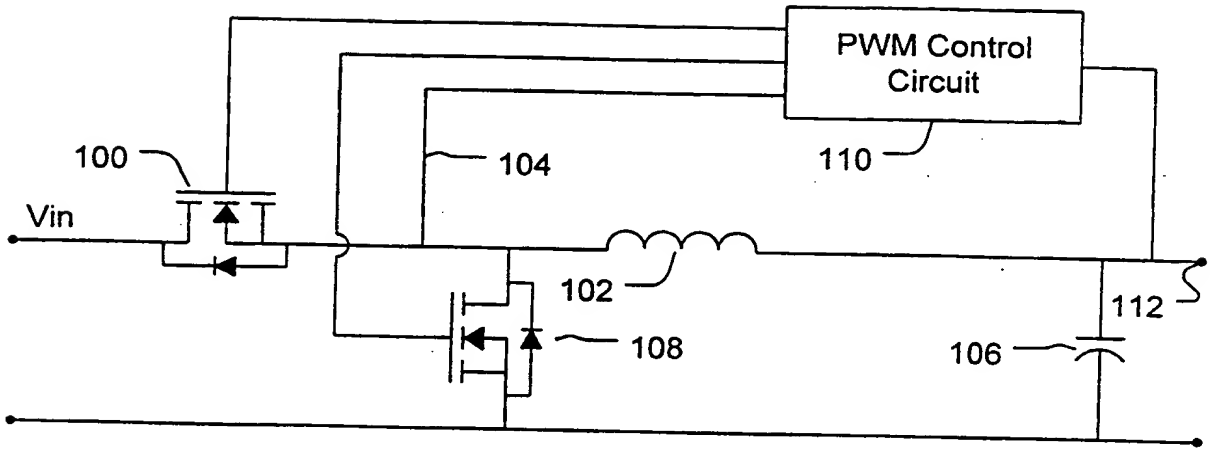

Fig. 8a

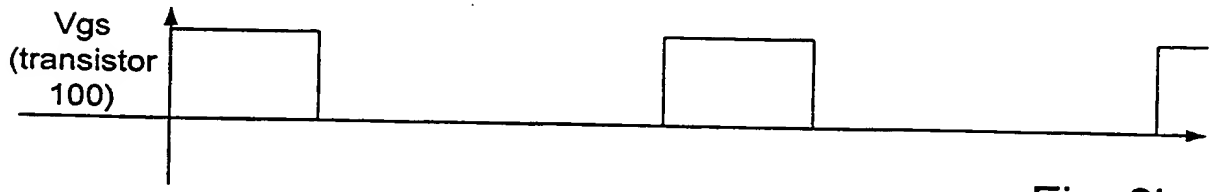

Fig. 8b

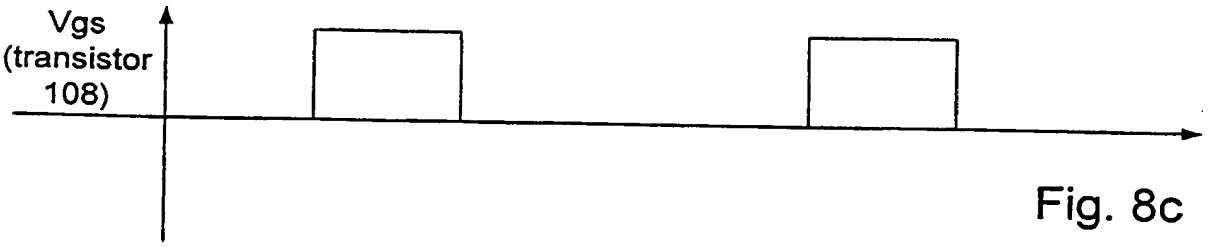

Fig. 8c

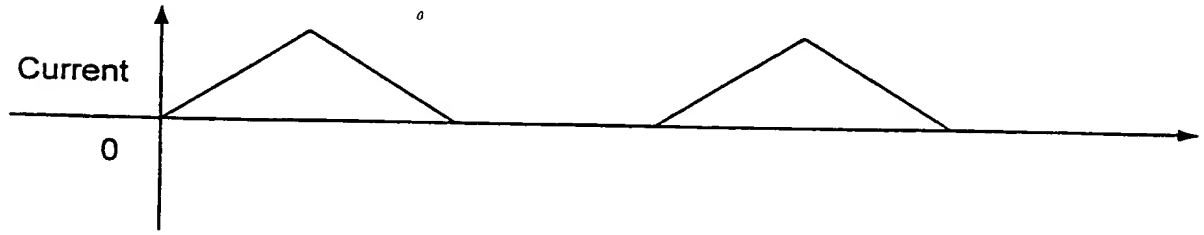

Fig. 8d

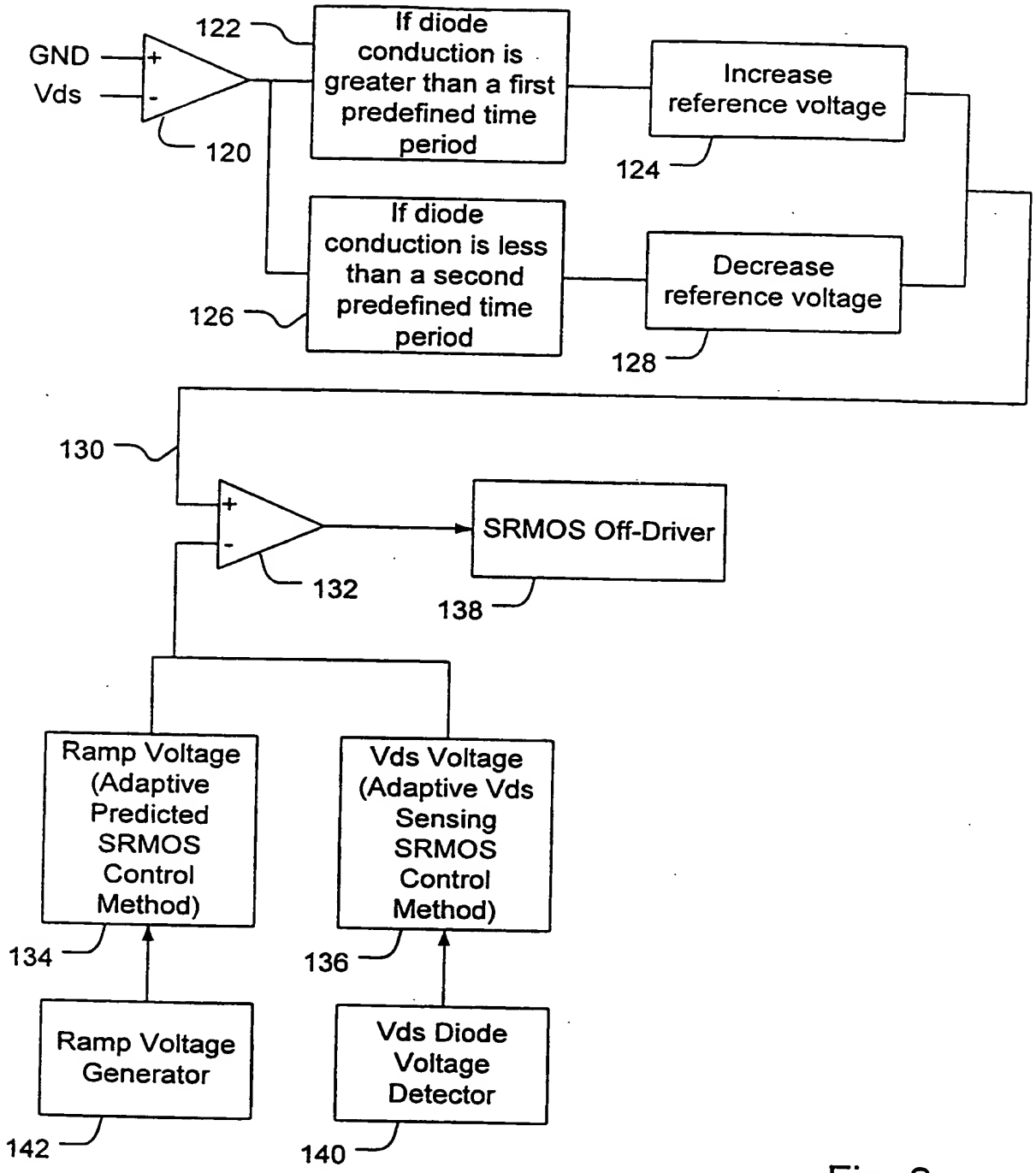
GND
Vds
+
-
120
122
If diode conduction is greater than a first predefined time period
Increase reference voltage
124
If diode conduction is less than a second predefined time period
126
Decrease reference voltage
128
130
+
-
132
SRMOS Off-Driver
138
Ramp Voltage (Adaptive Predicted SRMOS Control Method)
134
Vds Voltage (Adaptive Vds Sensing SRMOS Control Method)
136
Ramp Voltage Generator
142
Vds Diode Voltage Detector
140

Fig. 9

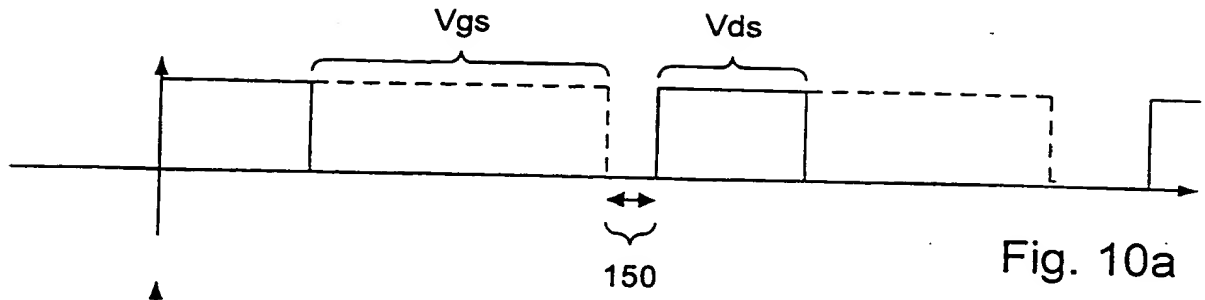

Fig. 10a

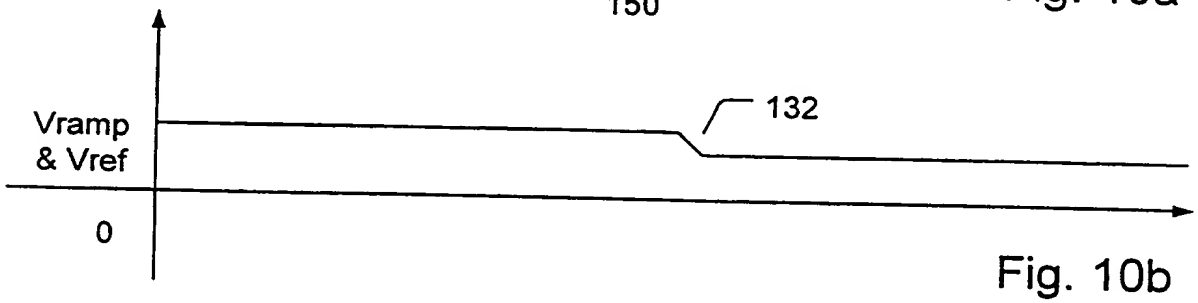

Fig. 10b

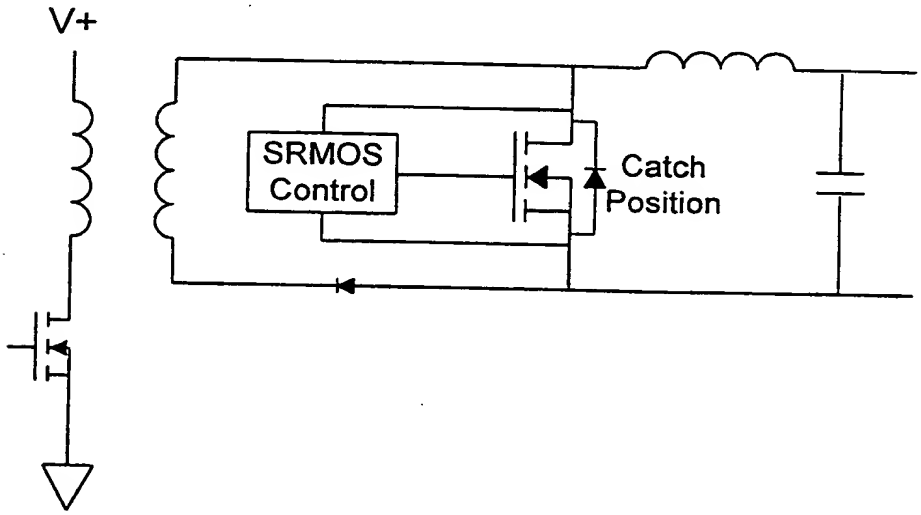

Fig. 11

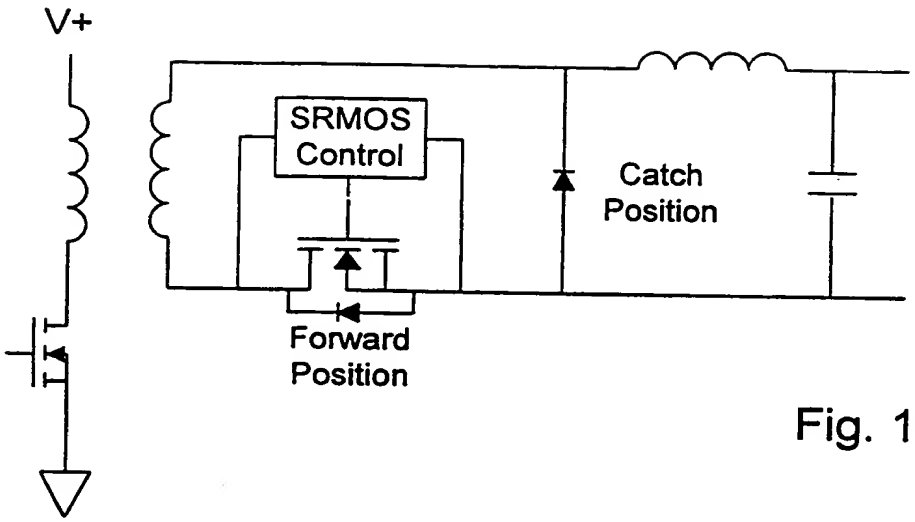
V+
SRMOS
Control
Catch
Position
Forward
Position

Fig. 12

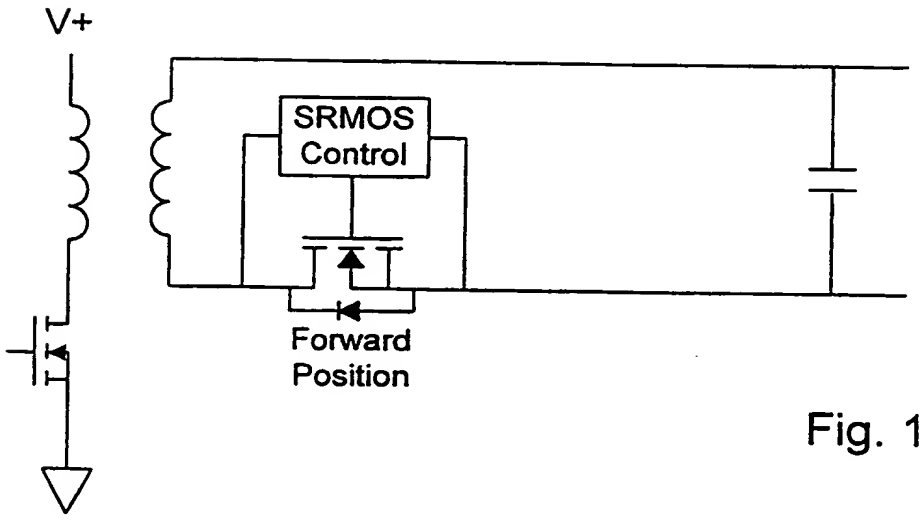
V+
SRMOS
Control
Forward
Position

Fig. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/11230

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H02M 7/217
US CL :363/89
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 363/89, 127

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, 5,523,940 A (WYMELENBERG) 04 JUNE 1996, (04/06/96) SEE ALL.	1-4, 21, 26-28
A	US 4,870,555 A (WHITE) 26 SEPTEMBER 1989, (26/09/89) SEE ALL.	1-46
A	US 5,430,640 A (LEE) 04 JULY, 1995, (04/07/95) SEE ALL.	1-46
A	US 5,424,932 A (INOU ET AL) 13 JUNE 1995, (13/06/95) SEE ALL.	1-46
A	US 5,528,480 A (KIKINIS ET AL) 18 JUNE 1996, (18/06/96) SEE ALL.	1-46
A,P	US 5,742,491 A (BOWMAN ET AL) 21 APRIL 1998, (21/04/98) SEE ALL.	1-46

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 06 JULY 1998	Date of mailing of the international search report 19 AUG 1998
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer JEFFREY STERRETT Telephone No. (703) 308-1632

Form PCT/ISA/210 (second sheet)(July 1992)★ . . .